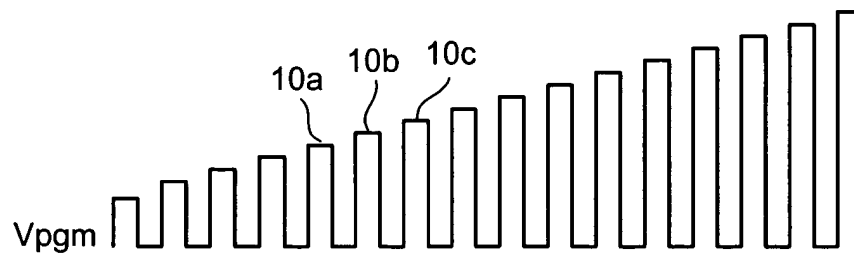


Fig. 1



# of cells

Fig. 2

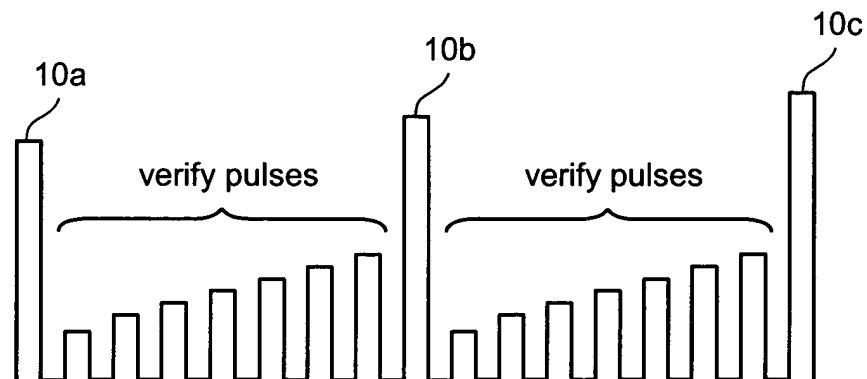
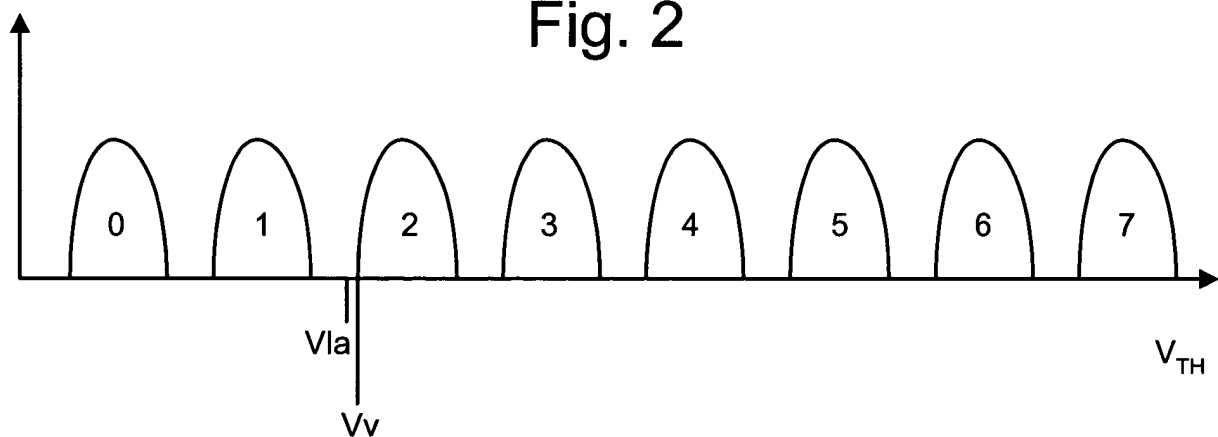


Fig. 3

**Fig. 4**

The diagram illustrates a memory system architecture with the following components and connections:

- Host (35)**: Connected to the **Controller (27)** via a bidirectional arrow.
- Controller (27)**: The central management unit, connected to several other blocks.
  - It sends a **Control/Status** signal (33) to the **Steering Gates Decoders and Drivers (21)**.
  - It receives a **Control/Status** signal (31) from the **Select Gates (Word Lines) Decoders and Drivers (19)**.
  - It is connected to a **Bus (25)**, which in turn connects to the **Select Gates (Word Lines) Decoders and Drivers (19)**.
  - It receives a **Control/Status** signal (29) from the **Bit Line Decoder, Drivers and Sense Amplifiers (22)**.
  - It receives an input signal (41) from the bottom.
- Steering Gates Decoders and Drivers (21)**: Receives control signals from the Controller and the memory array (23).
- Select Gates (Word Lines) Decoders and Drivers (19)**: Receives control signals from the Controller and the memory array (17), and is connected to the memory array via a bidirectional arrow (11).
- memory array (11)**: The central data storage component, connected to the other three main blocks via bidirectional arrows (23, 17, 15).
- Bit Line Decoder, Drivers and Sense Amplifiers (22)**: Receives control signals from the Controller and the memory array (15), and outputs a **Read** signal (13) back to the memory array.

This diagram shows a cross-sectional view of a semiconductor device. A central channel region (103) is defined by a gate stack (105) and is flanked by side gates (55, 56 on the left and 57, 58 on the right). The device is built on a substrate (45) with a top layer (92). The channel region is separated from the side gates by a spacer (99). The side gates are formed by a gate stack (55, 56) and a side gate layer (57, 58). The device is also surrounded by a passivation layer (81, 83). The channel region is labeled 103, the gate stack is 105, the side gates are 55, 56, 57, 58, the spacer is 99, the top layer is 92, the substrate is 45, and the passivation layer is 81, 83. The channel region is also labeled 49 and 51. The side gates are also labeled 47. The channel region is also labeled T1-left, T2, and T1-right.

Left Steering Gate

Select Gate (Word Line)

Right Steering Gate

55' 81' 56' 49' BL left

T1-Left T2

92' 99' 57' 83' 58' 51' BL right

T1-Right

Title: CHARGE PACKET METERING FOR COURSE/FINE PROGRAMMING OF NON-VOLATILE MEMORY

Applicants: Guterman, et al.

Docket No.:

SAND-01016US0

Appl. No.: Unknown

Atty:

Burt Magen

Filing Date: January 27, 2004

Phone:

(415) 369-9660

Express Mail No.: EV 391 867 405 US

Fig. 8

FUNCTION BEING PERFORMED ON CELL	SELECT GATE (WORD LINE)	LEFT BIT LINE (BL - LEFT)	LEFT STEERING GATE	RIGHT STEERING GATE	RIGHT BIT LINE (BL-RIGHT)
(1) UNSELECTED ROW (2) ERASE (TO WORD LINE) (3) READ LEFT FLOATING GATE (4) READ RIGHT FLOATING GATE (5) PROGRAM LEFT FLOATING GATE (6) PROGRAM RIGHT FLOATING GATE (7) NO PROGRAM IN SELECTED ROW	0 $V_E$ $V_{SR}$ $V_{SR}$ $V_{SP}$ $V_{SP}$ $V_{SP}$	X 5 0 1 5 0 0 5	X 0 $V_M$ $V_{BR}$ $V_P$ $V_{BP}$ X X	X 0 $V_{BR}$ $V_M$ $V_{BP}$ $V_P$ X X	X 5 1 0 0 5 0 5
(8) ERASE (TO CHANNEL) [WITH VOLTAGES OF BOTH THE p-well AND n-well EQUAL TO $V_E$ , AND THE SUBSTRATE AT ZERO VOLTS]	$V_{SE}$	FLOAT	0	0	FLOAT

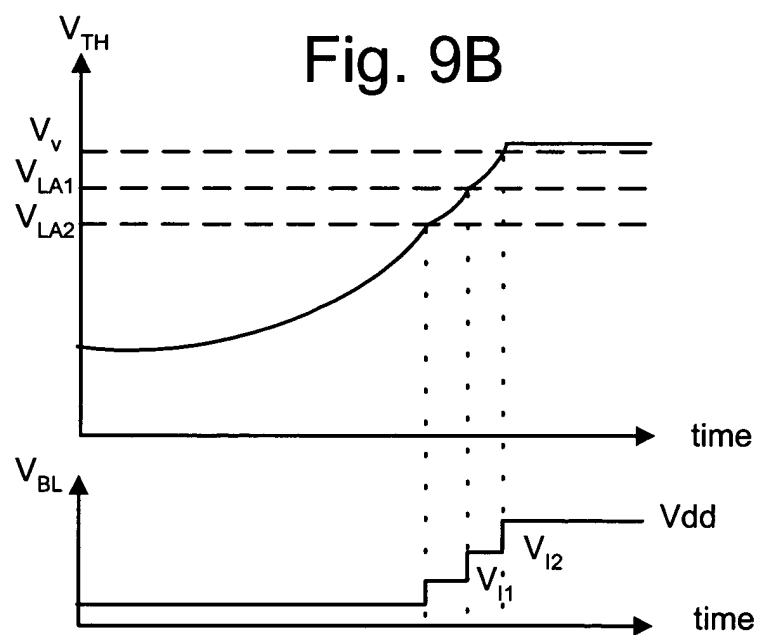
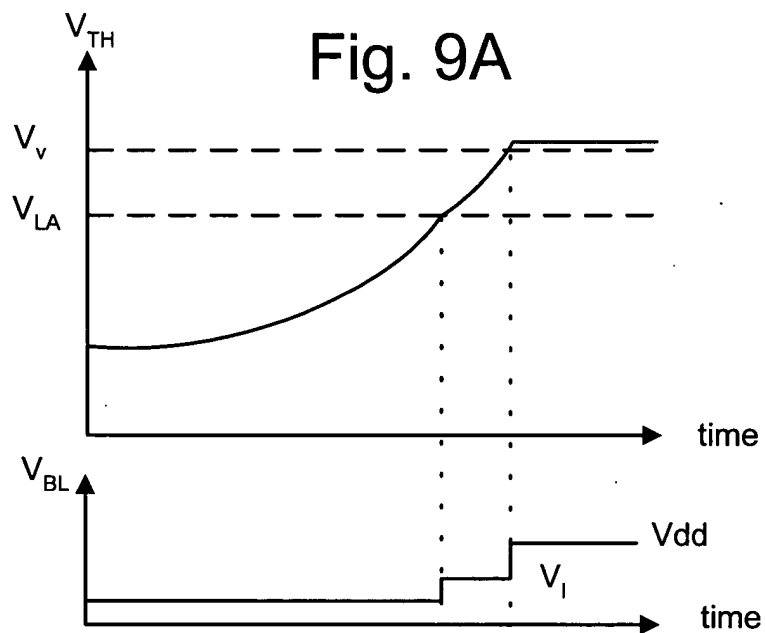
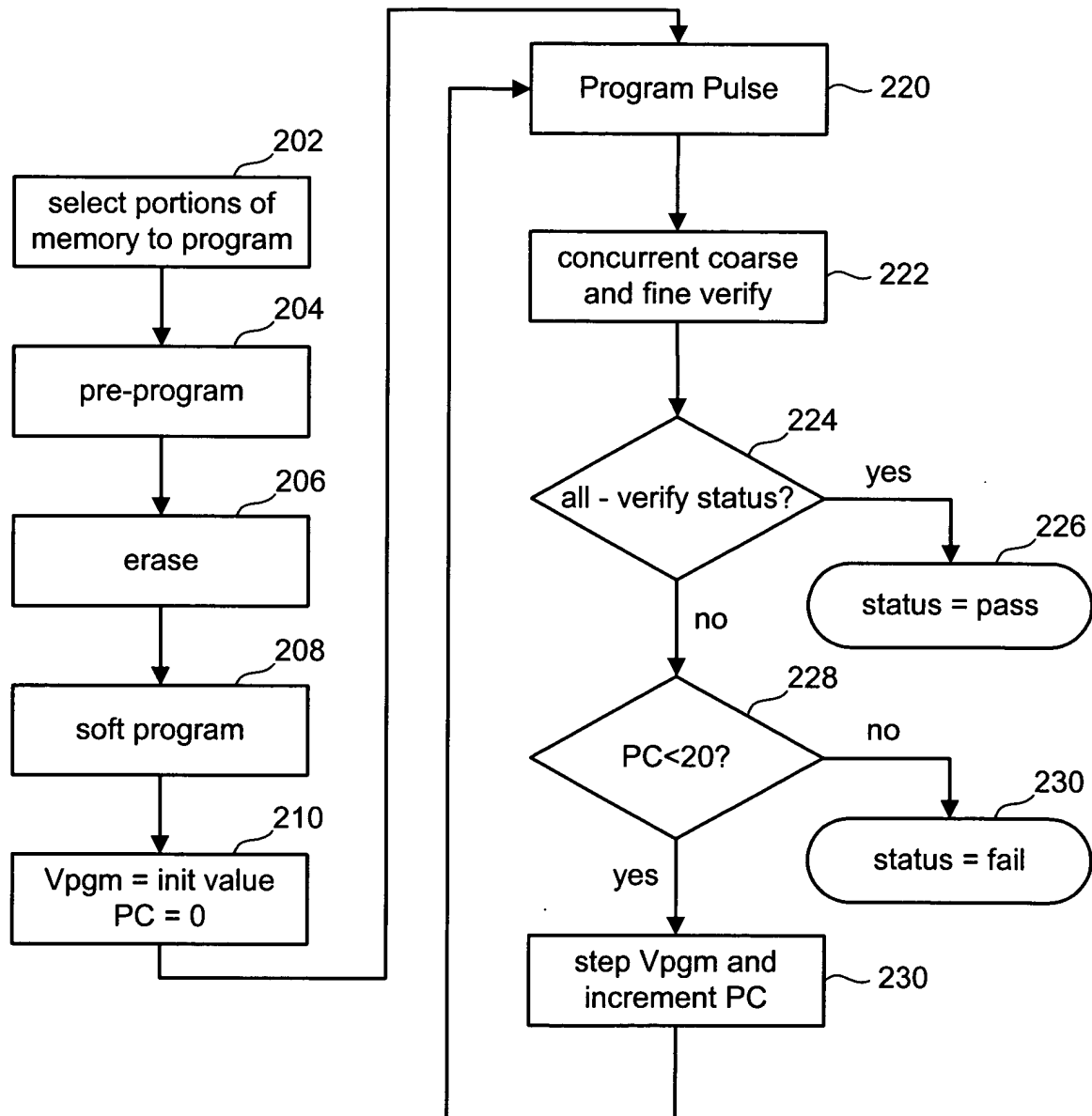


Fig. 10



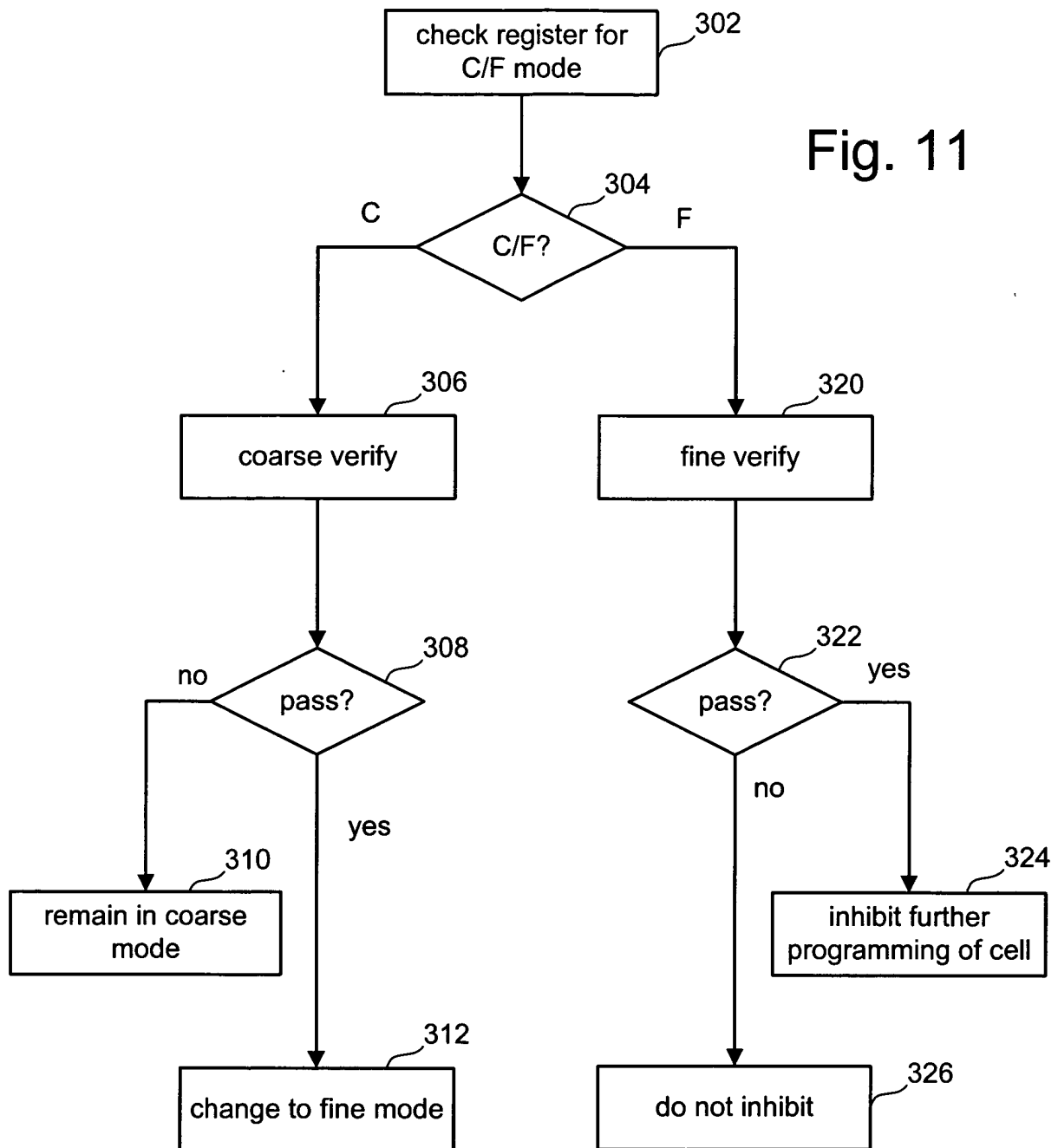


Fig. 12

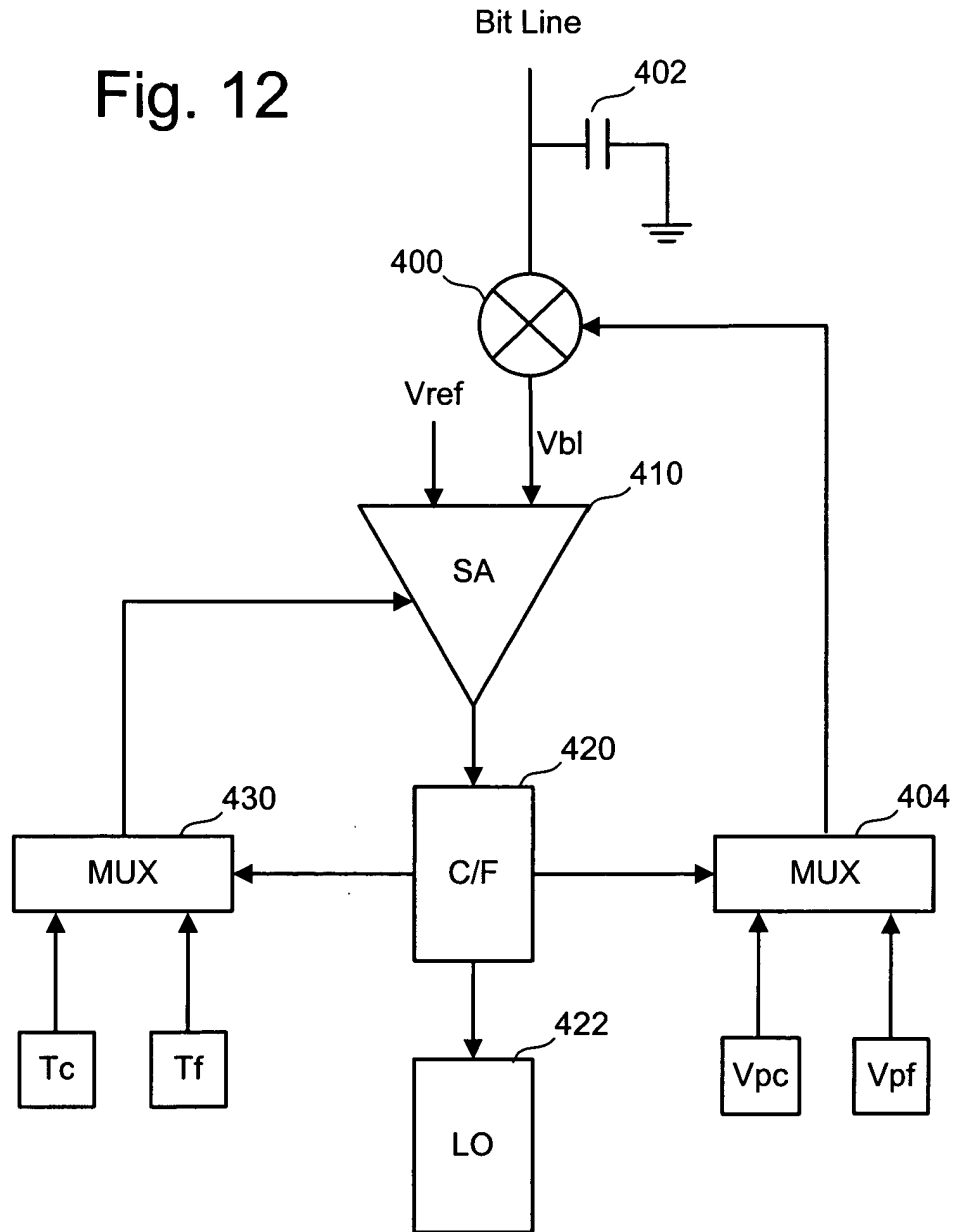


Fig. 13

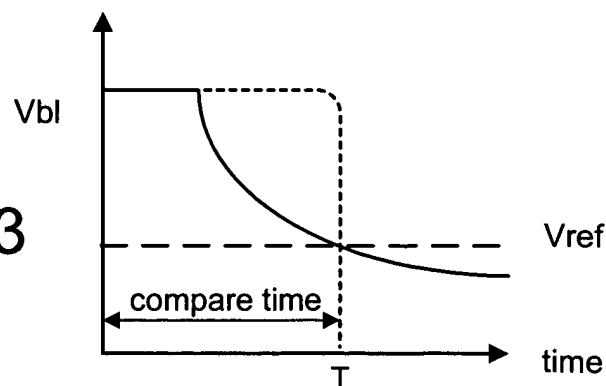




Fig. 14

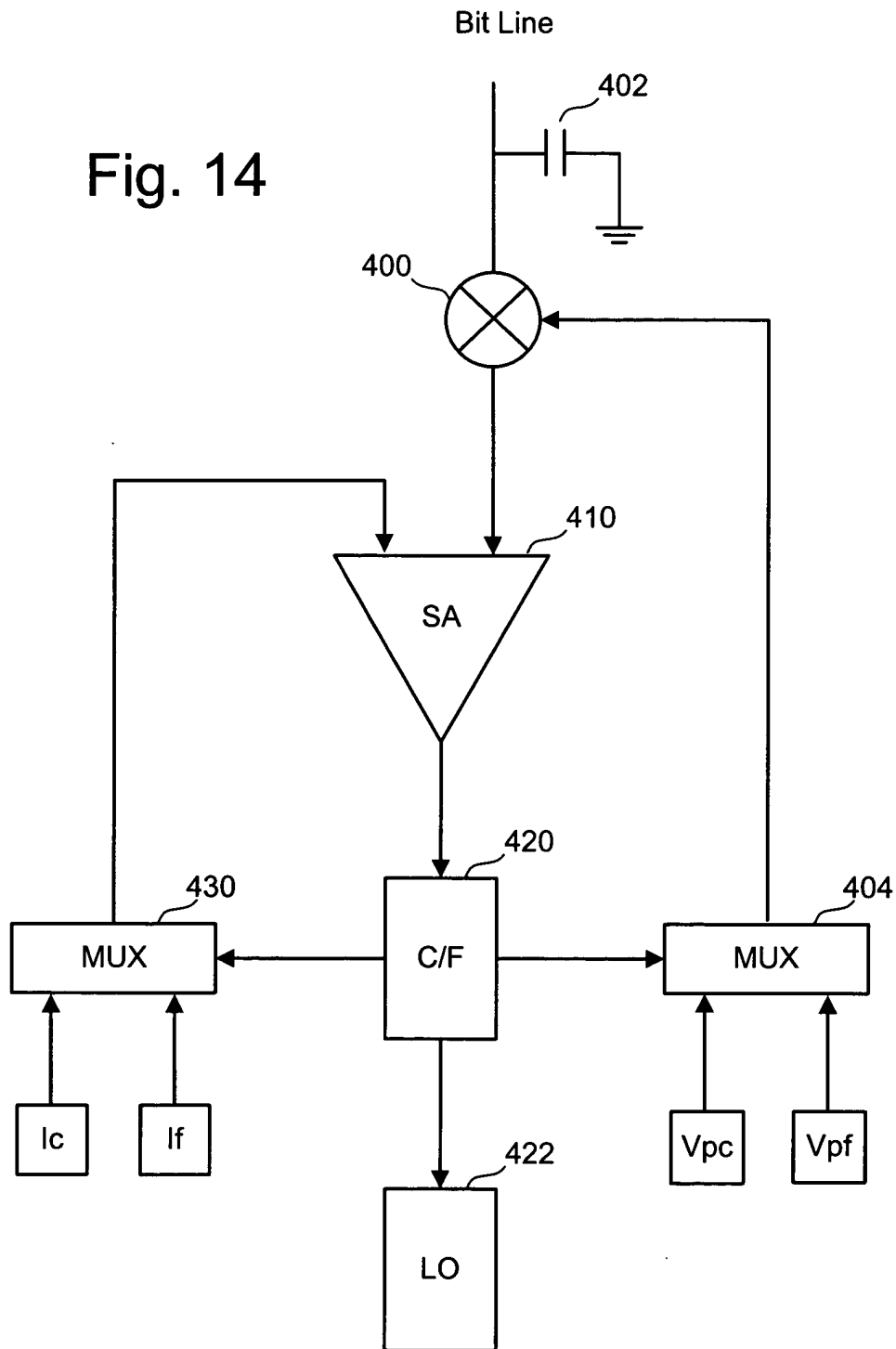


Fig. 15

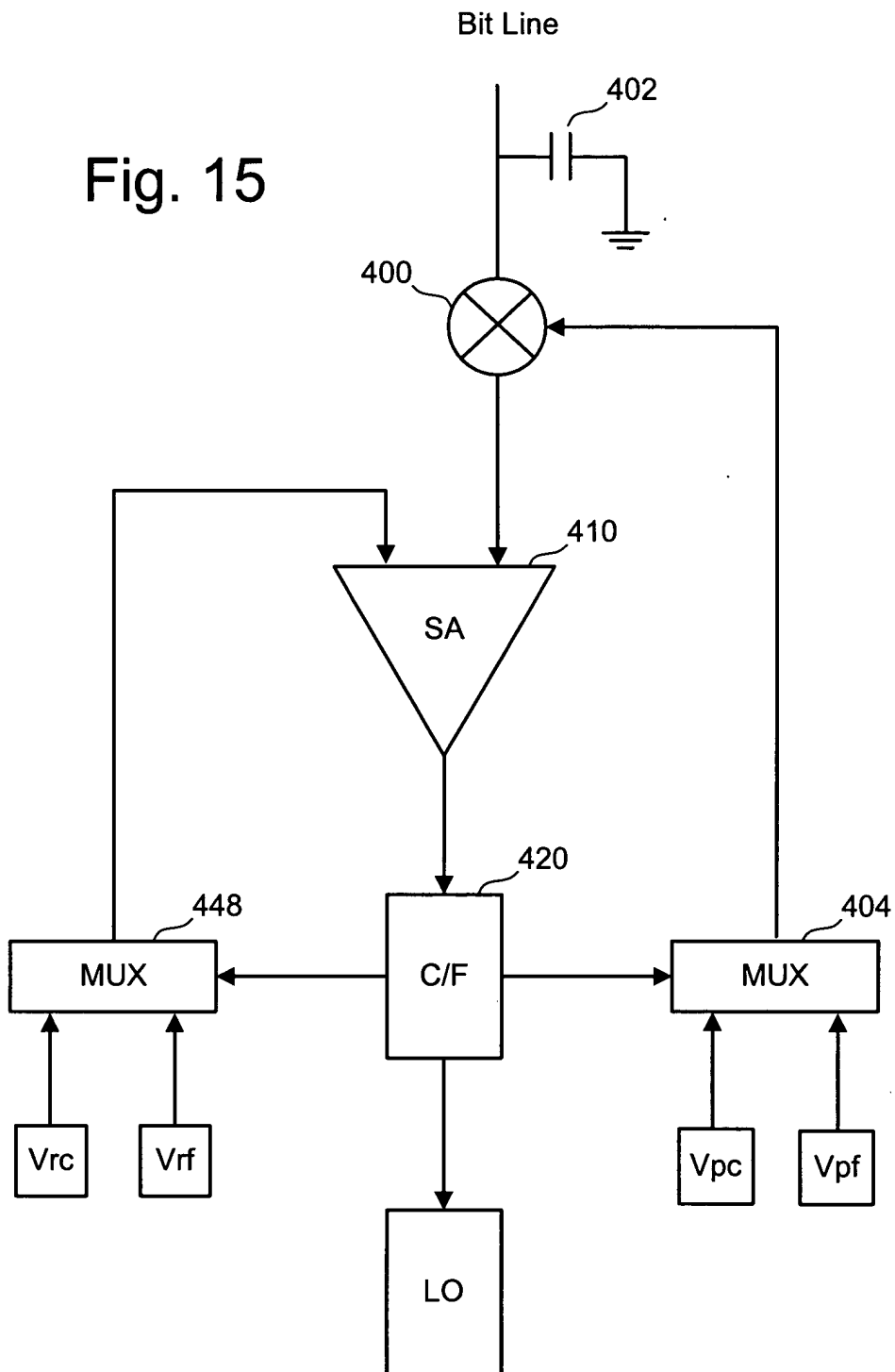


Fig. 16

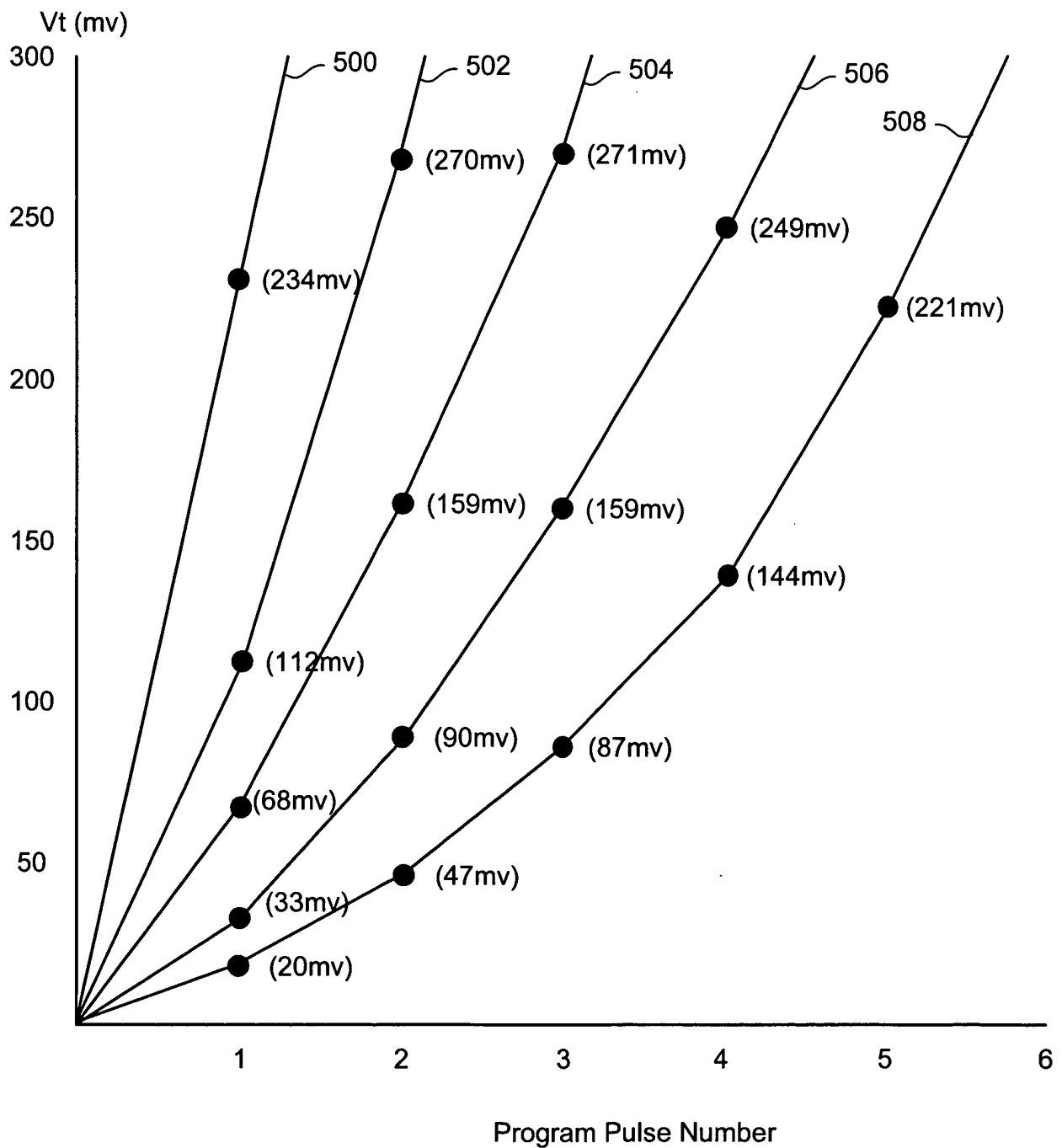


Fig. 17

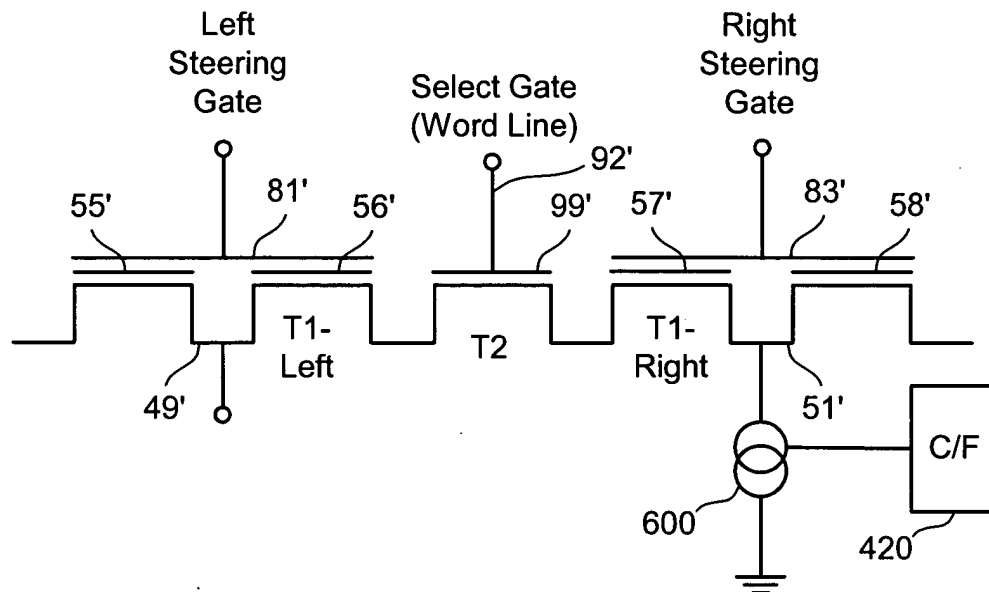


Fig. 18

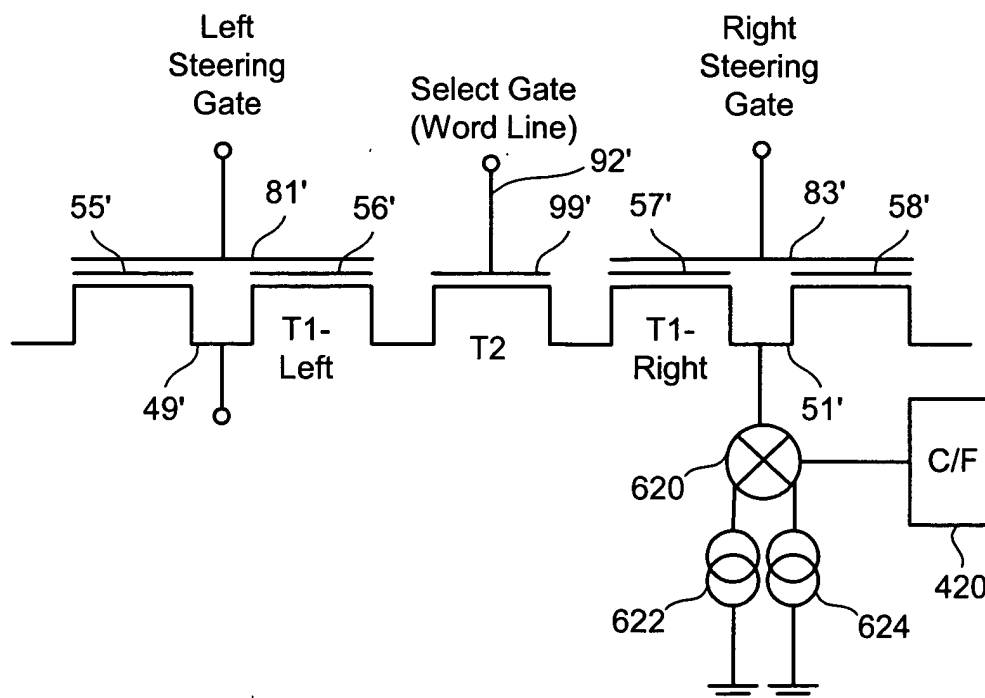


Fig. 19

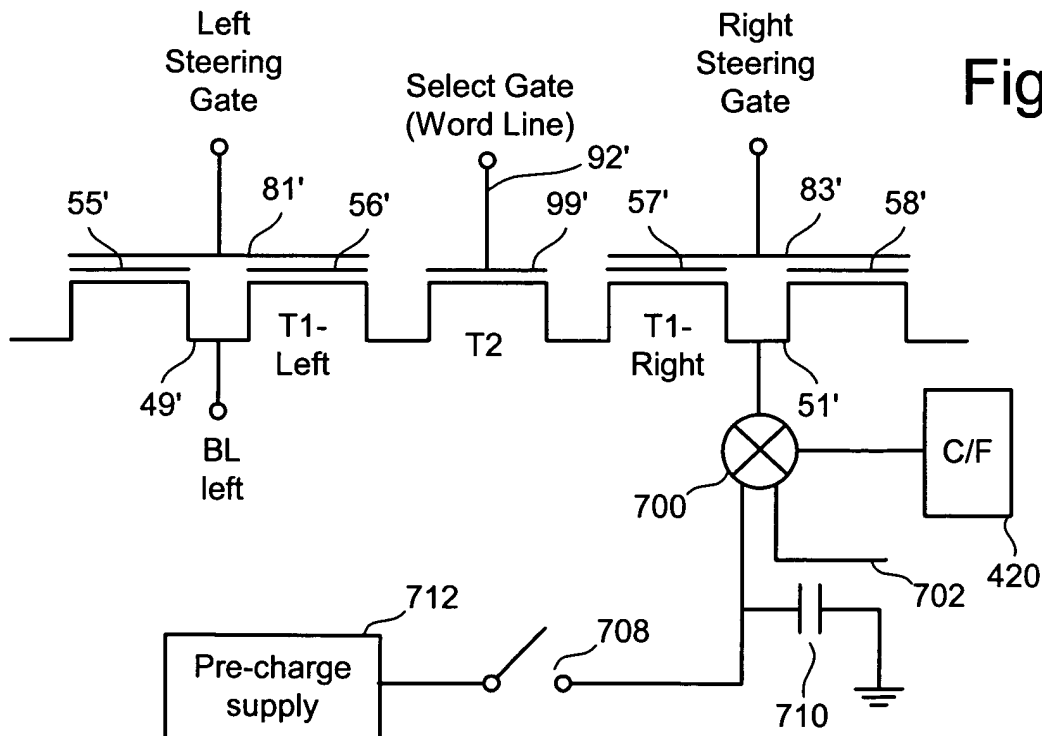
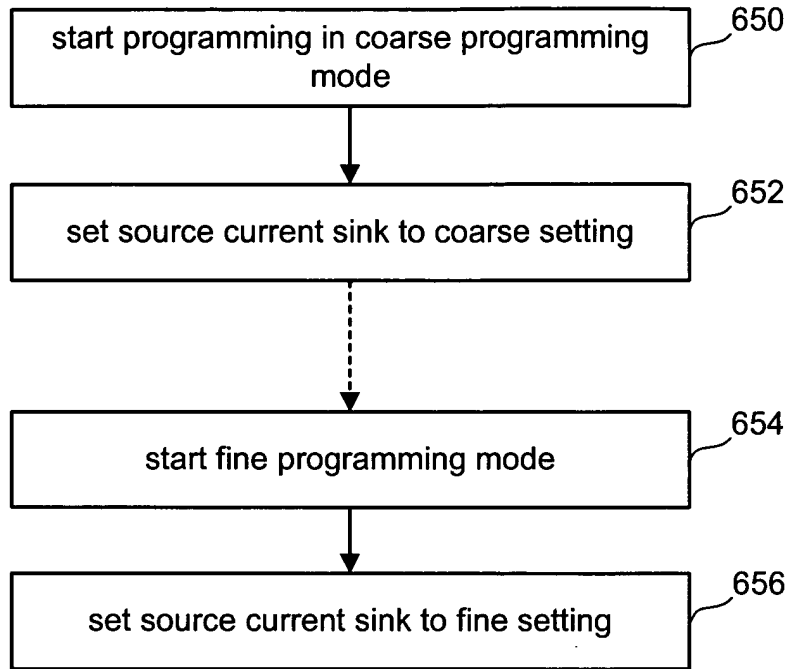


Fig. 20

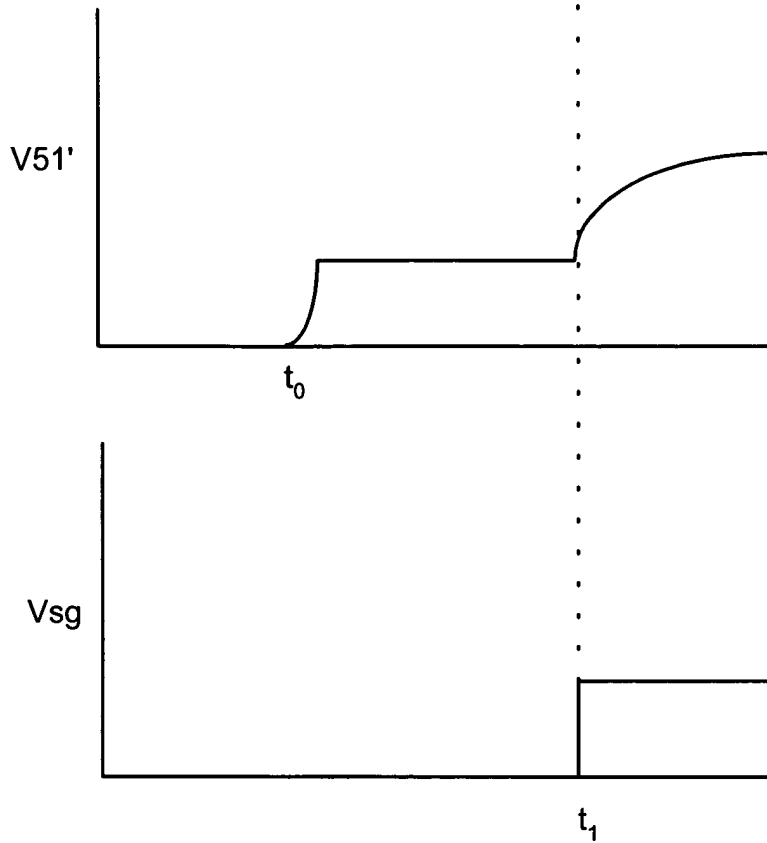


Fig. 21

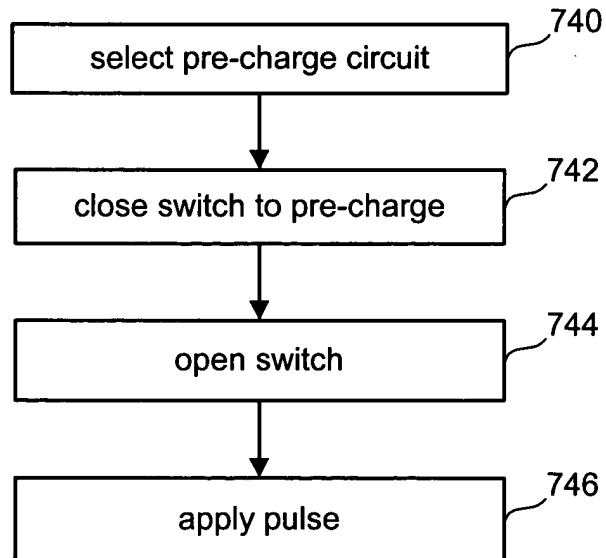


Fig. 22

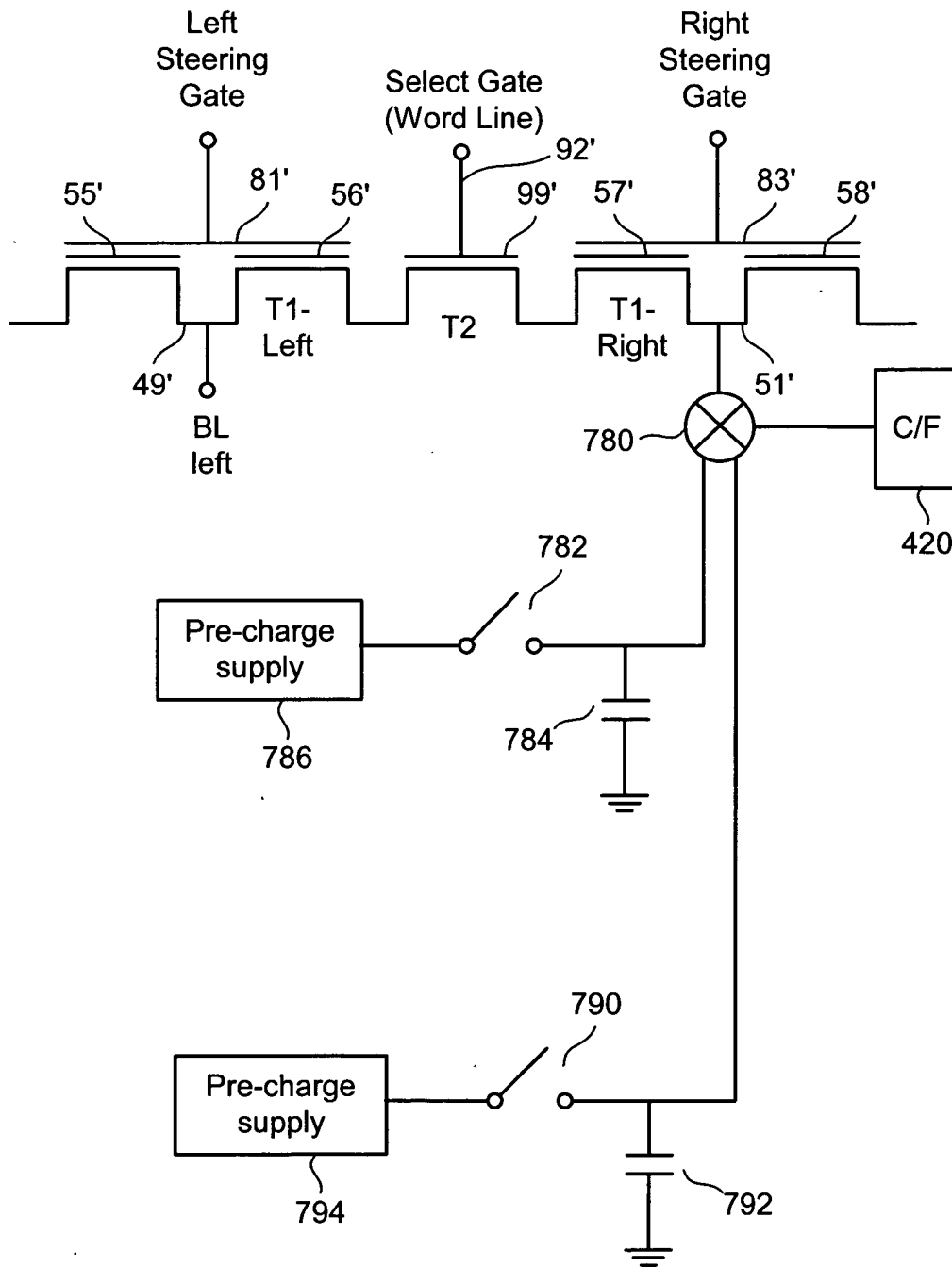


Fig. 23

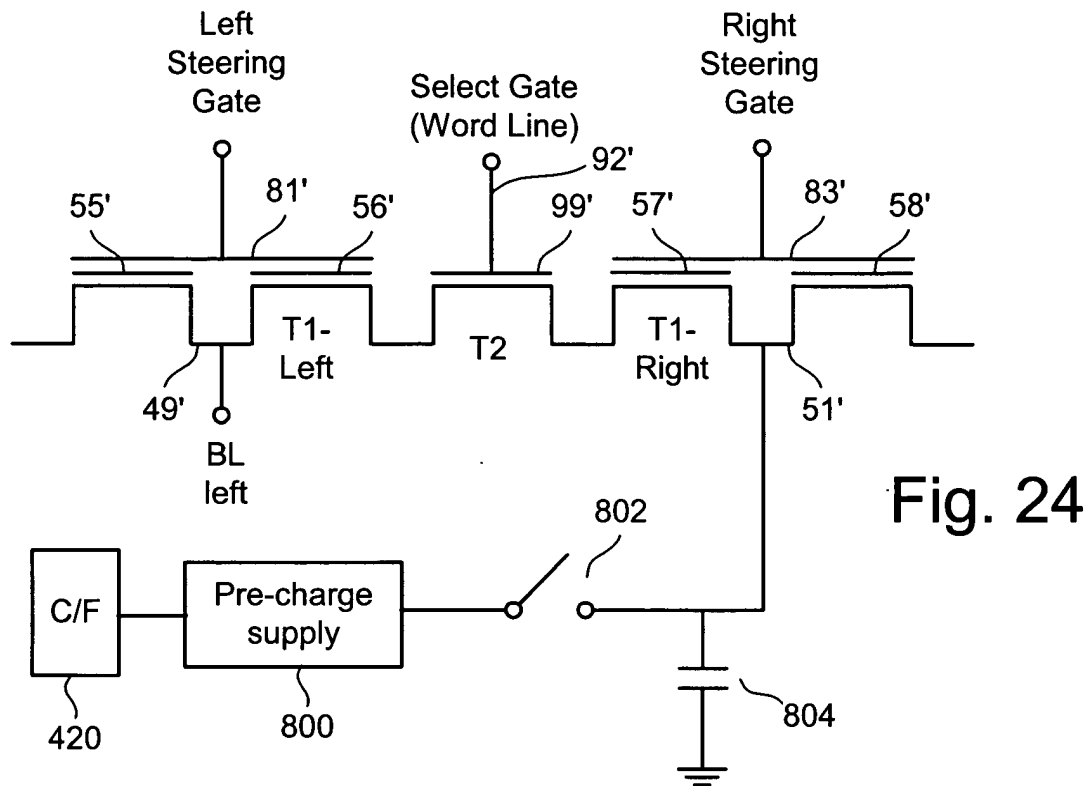


Fig. 24

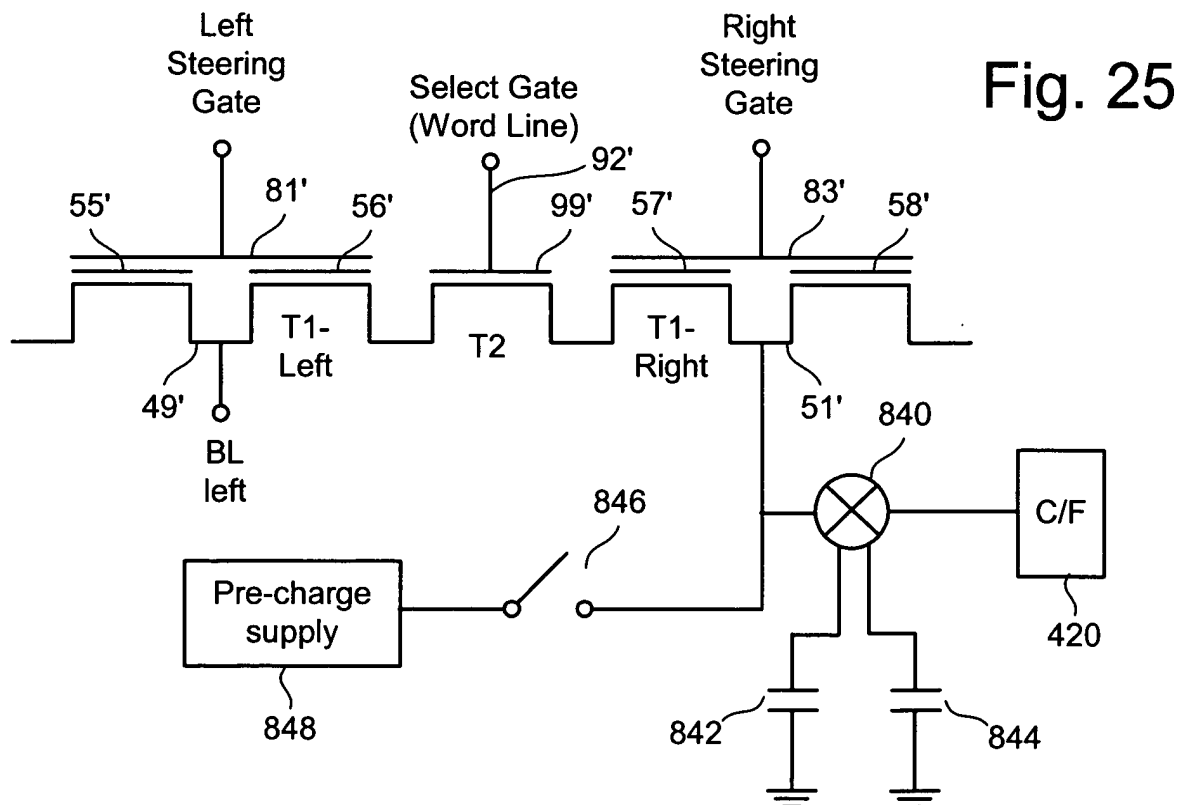


Fig. 25